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REMARKS

Claims 1, 9, and 10 are pending in this patent application and are allowed.

In a telephonic interview with Applicants' representatives conducted on February 7, 2002, Examiner Bui requested that certain portions of the specification, in particular on pages 6-9, be amended to remove references to claims 1-8, which are cancelled.

In accordance with the discussion during the telephonic interview, Applicants have amended the portions of the specification on pages 6-9 to eliminate the noted references to the claims. No new matter has been added. Applicants respectfully request that this amendment be entered because it (1) is necessary for proper description and (2) does not require a substantial amount of additional work on the part of the Office.

During the telephonic interview, Examiner Bui also indicated that the Declaration and Power of Attorney for this application was not in the PTO file and could not be located.

Applicants enclose herewith a true copy of the executed Declaration and Power of Attorney, along with a stamped receipt from the PTO indicating that this document was filed on May 31, 2000.

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Should the Examiner believe that any issues remain to be resolved, the Examiner is hereby invited to contact the undersigned to discuss the same.

Respectfully submitted,

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Enclosure:

Appendix (pp. 7-10)
Declaration and Power of Attorney

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APPENDIXVERSION WITH MARKINGS TO SHOW CHANGES MADEIN THE SPECIFICATION:

The paragraph extending from page 6, line 26 to page 7, line 11 is amended as follows:

[In Claim 1 of the present invention,] In a package board according to a first aspect of the invention, the soldering pads on the IC chip side surface of the package board are small, so the rate of the metallic portion occupied by those soldering pads is also small. On the other hand, the soldering pads on the mother board side surface of the package board are large, so the rate of the metallic portion occupied by those soldering pads is also large. This is why a dummy pattern is formed between conductor circuit patterns on the IC chip side surface of the package board thereby to increase the metallic portion and adjust the rate of the metallic portion between the IC chip side surface and the mother board side surface of the package board so as to protect the package board from warping. The dummy pattern mentioned above does not have any functional meaning such as an electrical connection and a capacitor. It just means a pattern formed mechanically.

The paragraph extending between lines 12-25 on page 7 is amended as follows:

[According to the invention defined in Claim 2,] In a package board according to a second aspect of the invention, the soldering pads on the IC chip side surface of the package board are small. Thus, the metallic portion occupied by the soldering pads is less than that of the mother board side surface of the package board, where the soldering pads are large and the metallic portion occupied by the soldering pads is large. This is why a dummy pattern is formed at the outer periphery of each conductor circuit on the IC chip side surface of the

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package board thereby to increase the metallic portion thereon and adjust the rate of the metallic portion on the package board surface between the IC chip side and the mother board side. This metallic dummy pattern is also effective to improve the mechanical strength of the outer periphery of the package board, as well as protect the package board from warping.

The paragraph extending from page 7, line 26 to page 8, line 5 is amended as follows:

[According to the package board defined in Claim 3,] In a package board according to a third aspect of the invention, a power supply layer and/or a ground layer is formed as an inner layer conductor circuit formed under an insulating layer that supports the outermost layer conductor circuits. Then, a via-hole is connected directly to the second conductor circuit and a solder bump is formed in the via-hole. It is therefore not necessary to provide a wire for connecting the power supply layer or the ground layer to the soldering bumps. Consequently, the package board is free of any noise to be mixed in wires.

The paragraph extending between lines 6-15 on page 8 is amended as follows:

[According to the package board defined in Claim 4,] In a package board according to a fourth aspect of the invention, a power supply and/or a ground layer is formed as the second conductor circuit disposed under the second interlaminar resin insulating layer that supports the conductor circuits formed in the outermost layer. A via-hole is connected directly to the second conductor circuit and a soldering bump is formed in the via-hole. It is therefore not necessary to provide a wire for connecting the power supply layer or the ground layer to the soldering bumps. Consequently, the package board is free of any noise to be mixed in wires.

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The paragraph extending between lines 16-27 on page 8 is amended as follows:

[According to the package board defined in claims 5 and 6,] In a package board according to a fifth aspect of the invention, each land and each pad are formed integrally and connected directly to each other without using a wire. It is thus possible to shorten the transmission path provided between upper and lower conductor layers, as well as to reduce the connecting resistance significantly. In addition, since the land and the pad are connected directly to each other without using a wire, no stress is concentrated at a joint between wiring and land, as well as at a joint between wiring and pad. It is thus possible to protect the package board from breaking of a wire to be caused by a crack generated by such concentrated stress.

The paragraph extending from page 8, line 28 to page 9, line 11 is amended as follows:

[According to the package board defined in Claim 7,] In a package board according to a sixth aspect of the invention, a soldering bump is formed in a via-hole, so that each soldering bump is connected directly to a via-hole. Therefore, even when the package board is cracked, it is prevented that breaking of a wire occurs between the soldering bump and the via-hole. In other words, the conventional package board, where a soldering pad is connected to a via-hole through a wire and a soldering bump is formed on a soldering pad, cannot avoid crack-caused breaking of a wire connecting via-holes to soldering pads. A soldering bump is thus disconnected from a via-hole due to such a crack generated inside the package board. The package board defined in [Claim 7] this aspect of the invention, however, is completely protected from breaking of a wire caused by such a crack.

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The paragraph extending between lines 12-23 of page 9 is amended as follows:

[According to the package board defined in Claim 8,] In a package board according to
a seventh aspect of the invention, a soldering bump is formed in a via-hole, so that each
soldering bump is connected directly to each via-hole. It is thus possible to prevent breaking
of a wire between a soldering bump and a via-hole even when the package board is cracked.
Such a soldering bump is also formed in a plurality of via-holes respectively in this case. It is
possible to utilize a fail-safe, since the soldering bump can be connected to another via-hole
when one of the via-holes is disconnected from the soldering bump. In addition, since a
soldering bump is formed on a plurality of via-holes, a soldering bump can be formed larger
to each via-hole.

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